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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,603	03/29/2004	David H. Shen		9709

7590
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EXAMINER

MAI, TAN V

ART UNIT	PAPER NUMBER
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2193

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09/23/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,603	SHEN, DAVID H.	
	Examiner	Art Unit	
	Tan V. Mai	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-11 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9-11,15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. It is noted that the "Listing of Claims" is NOT standard. For example,

"2. (Original)" should be "2. (Previously amended)"; and

"8. (Original)" should be "8. (Cancelled)".

3. Claims 1-7, 9-11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasper et al, recorded reference.

Rejection grounds continue to be those set forth in the previous office action (Paper dated 4/5/10, paragraph 2).

4. Applicants' arguments filed on 7/8/10 have been fully considered but they are not persuasive.

Applicant, in his remarks, argues that:

"1. The disclosure as described in the specification, in the drawings and in the claims, the disclosed analog filter uses transconductance elements and each transconductance element performs filtering function as well as converting the input signal into a current. The outputs of the transconductance elements are coupled together to form a current summing node to sum the output currents. The

disclosure then uses a transimpedance to convert the output summed current into a filtered voltage output signal.

Kasper et al.'s patent uses traveling wave amplifier whose input and output signals are both of the same type, namely, **voltage signals**, specifically as written in Kasper et al's Claim 1, 'each of said first and second amplified electrical signals being an amplified replica of said input electrical signal'. In addition, Kasper et al's patent does **not** have a current summing node and summed output current. Therefore, it is not possible to couple a 'transimpedance element' to the output (303,403) of Kasper et al's patent to make the claimed invention of this disclosure as stated in the Action of April 5, 2010.

2. The disclosure as described in the specification, in the drawings and in the claims, the disclosed analog filter does not uses any artificial transmission lines and uses only one transmission delay line. In addition, this disclosure does not require any time synchronization of input and output signals.

In contrary to this disclosure, Kasper et al.'s patent uses **two** transmission delay lines one at the input of the traveling wave amplifier and one at the output of the

traveling wave amplifier, specifically, stated in Kasper's independent claims 1 and 12: 'said first and second amplification branches including an input artificial transmission line and an output artificial transmission line coupled to said input port and said output port, respectively'. It is well known in the art that traveling wave amplifiers require two transmission delay lines (real or artificial) in order to provide distributed amplification and time synchronization between input and output signals of the traveling wave amplifier.

3. Kasper et al.'s patent only has a forward propagation structure without any capability for a feedback of the output signal, thus can not provide any IIR filtering capability as described in this invention shown in Fig. 3 and related specification text.
4. This disclosure uses two or more transconductance elements and one transmission delay line to perform continuous-time filtering functions as well as converting voltage signals at the inputs of the transconductance elements to currents at the outputs of the transconductance elements. This disclosure uses continuous-time transconductance elements

and continuous-time transmission line delay elements to implement filtering functions in continuous time and without the need for sample and hold circuits. Shou et al's patent uses sampling and holding circuits, and digital multiplication coefficients to perform filtering functions. Because of its sampling and holding function, Shou et al's patent does not include continuous-time filtering and only works for low frequency input signals, specifically, for frequencies in the range of no more than a few hundred kHz as shown in Fig. 7 and related specification text. Shou et al's patent requires a significant amount of added sampling and holding circuits and the output filtered signal is only discrete-time versus this disclosure's continuous-time output filtered signal.

5. This disclosure uses one transmission delay line to delay an input signal and two or more transconductance elements to perform multiplication functions on delayed signals before converting filtered signals to currents to be summed at a current summing node which is finally converted to a filtered voltage signal by a transimpedance. The hybrid use of voltage and current modes allow this disclosure's

invention of generating delays with a transmission line and processing multiplications with transconductors.

Shou et al's patent instead performs all sample and hold, multiplication and summing functions in current mode. Specifically as shown in Fig. 8 and also described in Abstract of Shou et al's patent, a single voltage-to-current converter is used to first convert the input signal to an input current before performing discrete-time filter functions by the sampling and holding circuits then using multiple levels of adders to add the sampled currents before convert the added sampled current back to a voltage signal by a current- to-voltage converter.” (emphasis added).

With respect to the arguments, the examiner carefully reviews Applicants' specification, drawings (Figures. 2-3), claimed invention and the applied reference, Kasper et al.

First, Kasper et al do show, e. g. see Fig. 3, a device comprises: an input signal, electrical signal (340), transmission delay line (440), amplifiers (301-i) with have input electrodes I_i and output electrodes O_i and an output signal, electrical signal (350). It is obvious to a person in the art that “electrical signal” is the same as the claimed “input signal”/“current”. It is also obvious to a person in the art that the electrical signal (350)

is equivalent to the claimed “current summing node”. It is noted that Kasper et al do not the claimed “current to voltage” feature; however, a person having ordinary skill in the art should coupled that feature with electrical signal (350) for providing the voltage signal for desired application.

Second, Kasper et al show two transmission delay lines. The claim recites a transmission delay line. Therefore, Kasper et al do show the claimed “transmission delay line”. It is noted that Kasper et al do show all the claimed features of independent claim 1 except the “current to voltage” feature.

Third, the claims do not recite the

“a feedback of the output signal, thus can not provide any IIR filtering capability as described in this invention shown in Fig. 3 and related specification text.”

Fouth, the added language “continuous-time” has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). It is noted that

“analog” is equivalent to “continuous-time.” Shou et al's patent is art of interest. It is not an applied reference in the rejection.

Fifth, Shou et al's patent is art of interest. It is not an applied reference in the rejection.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock, Jr., can be reached on (571) 272-3759. The fax phone

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number for the organization where this application or proceeding is assigned is:

Official (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

/Tan V Mai/
Primary Examiner, Art Unit 2193